eExam Question Bank

Coursecode:

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Question Type	Question	A	B	C	D	Answer	Remark
FBQ	The '_____' gate is a circuit which will give a high output if either, but not both, of its two inputs are high	Exclusive-OR					eExam
FBQ	_____ converts one type of coded information to another form	Decoder					eExam
FBQ	The time required by a sector to reach below the read / write head of a disk is reffered to as _____	latency time					eExam
FBQ	A Boolean _____ is defined as an algebraic expression formed with the binary variables, the logic operation symbols, parenthesis, and equal to sign.	function					eExam
FBQ	A _____ is an electronic circuit which produces a typical output signal depending on its input signal.	logic gate					eExam
FBQ	_____ _Register specifies the address of the memory location from which the data or instruction is to be accessed	Memory Address					eExam
FBQ	Floating-point numbers are often represented in _____ forms.	normalised					eExam

☐								
☐	FBQ	The _____ code guards against the errors of two bits in SEC codes	SEC-DED					eExam
☐	FBQ	_____ is a binary cell, which can store a bit of information and which in itself is a sequential circuit.	Flip-flop					eExam
☐	FBQ	Control Instructions are used for testing the status of computation through _____	Processor Status Word					eExam
☐	FBQ	A _____ instruction causes a jump to the new instruction to be executed.	branch					eExam
☐	FBQ	_____ addressing mode is used to initialise the value of a variable.	immediate					eExam
☐	FBQ	A _____ connects multiple input lines to a single output line.	Multiplexer					eExam
☐	FBQ	The von Neumann machine uses a _____ program concept	stored					eExam
☐	FBQ	In Displacement Addressing the operand is stored in the _____ memory	virtual					eExam
☐	FBQ	The _____ Signal causes micro-operations to be performed	Master clock					eExam
☐	FBQ	In digital computers, there are _____ types of micro-operations	4	four				eExam
☐	FBQ	_____ Addressing Scheme is employed to relocate the program in the memory especially in a multiprogramming environment	Base					eExam

	FBQ	circuits use flip-flops and their status can change only at discrete instants.	Synchronous					eExam
	FBQ	Sequential circuits are logic circuits whose present depends on the past inputs.	output					eExam
	FBQ	The analytical engine is on display at the museum at London	science					eExam
	FBQ	An Asynchronous Counter is also referred to as a counter	ripple					eExam
	FBQ	Time is the minimum time lapse between two consecutive read requests .	Cycle					eExam
	FBQ	The amount of information which can be transferred between CPU and memory depends on the size of the connecting the two	BUS					eExam
	FBQ	The _-generation computers started with the advent of transistors	second					eExam
	FBQ	An input/output system also called I/O components allows data input and of the results in proper format and form.	reporting					eExam
	FBQ	The outputs of all gates are low if any of the inputs are high.	NOR					eExam
	FBQ	Interrupts are mainly used for improving the of processing.	efficiency					eExam
	FBQ	Register is a register which contains the data to be written in the memory .	Buffer					eExam

☐								
☐	FBQ	Magnetic tapes and _____ were used as secondary memory	Magnetic drums					eExam
☐	FBQ	A _____ is a two-state device made from silicon	transistor					eExam
☐	FBQ	Electronic Numerical Integrator and Calculator (ENIAC) was programmed _____	manually					eExam
☐	FBQ	In _____ register, instructions are loaded before their execution	Instruction					eExam
☐	FBQ	_____ keeps track of the instruction that is to be execute next, after the execution of an on-going instruction	Program Counter					eExam
☐	FBQ	_____ __is a useful operation which can be used for serial transfer of data	Shift					eExam
☐	FBQ	_____ operations are basically the binary operations which areperformed on the string of bits stored in the registers	Logic					eExam
☐	FBQ	A _____ instruction causes a jump to the new instruction to be executed.	branch					eExam
☐	FBQ	An arithmetic circuit is normally implemented using _____ adder circuits	parallel					eExam
☐	FBQ	_____ memories are alternate mass storage devices with huge capacity	Optical					eExam
☐	FBQ	_____ Addressing Scheme is used to address the consecutive locations of memory	Indexed					eExam

☐								
☐	FBQ	The constraint that a von Neumann machine could have one path between the main memory and the control unit is referred to as the von Neumann [ ]	bottleneck					eExam
☐	FBQ	A [ ] disk is a circular platter of plastic that is coated with magnetisable material	magnetic					eExam
☐	FBQ	[ ] memory can be accessed either by a word or by a bit-slice	Orthogonal					eExam
☐	FBQ	Bug is mainly used to indicate [ ] in computer programs	errors					eExam
☐	FBQ	Asynchronous sequential circuits may be regarded as [ ] circuits with feedback path.	combinational					eExam
☐	FBQ	The simplest model of instruction processing is a [ ] _-step process.	two					eExam
☐	FBQ	A von Neumann machine has only a [ ] between the main memory and the control unit (CU)	single path					eExam
☐	FBQ	The fifth generation computers emphasise massively [ ] Processing.	Parallel					eExam
☐	FBQ	A [ ] , which performs the addition of two bits, is called a half adder	combinational circuit					eExam
☐	FBQ	A [ ] bit is an extra bit added with binary data such that it makes the total number of 1's in the data either odd or even	parity					eExam

	FBQ	A program _____ is used for a fetch cycle in a typical CPU	counter					eExam
	FBQ	The CPU can be interrupted by providing a _____ line	control					eExam
	FBQ	The two basic functions of the control unit are microinstruction _____ and microinstruction execution	sequencing					eExam
	FBQ	The two widely used formats for microinstructions are _____ and _____	vertical , horizontal	horizontal, vertical				eExam
	FBQ	_____ occurs when the sum of two n digits numbersoccupies n+1 digit	an overflow					eExam
	FBQ	An octal system has _____ symbols	eight					eExam
	FBQ	The _____ by babbage was used for performing any mathematical operation automatically.	analytical engine					eExam
	FBQ	_____ made the first attempt towards automatic computing through inventing devices such as gears and chains	Blaise Pascal					eExam
	FBQ	A discrete component is a single self-contained _____ __.	transistor					eExam
	FBQ	The _____ is an arithmetical unit, which is capable of performing the four basic arithmetical operations.	Mills					eExam

☐	MCQ	The Mill is an arithmetical unit, which is capable of performing _____ basic arithmetical operations	two	three	four	five	C	eExam
☐	MCQ	Information is represented in a computer in the form of a _____ digit	Decimal	Binary	Hexadecimal	all of the options	B	eExam
☐	MCQ	Third generation computers mainly used _____ chips	large-scale integrated circuit	medium-scale integrated circuit	very large-scale integrated circuit	Small-scale integrated circuit	D	eExam
☐	MCQ	Which of the following is not one of the features on which the computer system family concept was implemented?	Simultaneous access of data in higher ends members	Increase in memory – CPU data paths	Increased complexity of the arithmetic logic unit	Reduced cost	D	eExam
☐	MCQ	The SEC-DED code guards against the errors of _____ bits in SEC codes	One	three	two	eight	C	eExam
☐	MCQ	A transistor is a two-state device made from _____.	Iron	Silicon	Potassium	none of the options	B	eExam
☐	MCQ	two major components are present in Wikes Design of a _____	macroinstruction	microinstruction	miniinstruction	megainstruction	B	eExam
☐	MCQ	A Von Neuman machine has how many paths between the main unit and the control unit ?	Double path	Multiple Path	Tripple Path	Single Path	D	eExam
☐	MCQ	Using the laws of Boolean algebra, (A+B) + B can be simplified to be_____ .	(A.B)	(A+B)	(A'.B)	none of the options	A	eExam
☐	MCQ	Logic circuits whose present output depends on the past inputs are?	Sequential circuits	Bus	serial	Parallel	A	eExam
☐	MCQ	_____ is another name for The NOT gate	Inverter	Converter	Adder	Transistor	A	eExam
☐	MCQ	Which of the following is 10's Complement of 421 ?	576	578	577	579	A	eExam
☐	MCQ	The _____ of an operand is implied, in Stack Addressing Scheme	Flipflop	Address	Operand	Counter	B	eExam
☐	MCQ	The ENIAC could perform how many multiplications or additions per minutes respectively?	500 or 5000 respectively	3000 or 300 respectively	300 or 3000 respectively	5000 or 500 respectively	D	eExam

	MCQ	_____ invented a device, which consisted of lots of gears and chains and used to perform repeated addition and subtraction	Von Neumann	Charles Babbage	Blaise Pascal	None of the options	C	eExam
	MCQ	_____ Register is a register which receives the data from the memory	Memory Address	Memory Buffer	Program Counter	none of the options	B	eExam
	MCQ	A branch instruction is also known as _____ instruction	Slip	jump	hop	leap	B	eExam
	MCQ	Evaluation-Stack Architecture are _____ address machines	two	one	Zero	three	C	eExam
	MCQ	_____ circuits' status can change only at discrete instants.	Isochronous	Synchronous	Asynchronous	All of the options	B	eExam
	MCQ	Requiring two memory references to fetch the operand is a disadvantage of _____ addressing scheme	Indirect	indexed	register indirect	Stack	A	eExam
	MCQ	The address capability of _____ addressing scheme is determined by the size of the register	register	stack	register indirect	indirect	C	eExam
	MCQ	The address of an operand is implied in _____ Addressing Scheme	register	indirect	direct	Stack	D	eExam
	MCQ	Instruction _____ determines the richness and flexibility of a machine	Width	Set	Length	All of the options	C	eExam
	MCQ	_____ acts as a buffer storage between the main memory and the CPU.	Program files	Data Register	Program	none of the options	B	eExam
	MCQ	Information in a computer is represented in the form of Binary digit called a_____	Data	code	Number	Bit	D	eExam
	MCQ	In bus arbitration technique, the ____ module first needs to control the bus and only after that can it request for an interrupt	Logic	I/O	Sequential	None of the above	B	eExam
	MCQ	In floating point number representation, the first part of the number is a signed fixed-point number is called _____	Mantissa	Fraction	Interger	Decimal	A	eExam

☐								
☐	MCQ	_____ is the decimal equivalent of the hexidecimal number (D6)	245	304	214	243	C	eExam
☐	MCQ	The Analytical Engine was a general purpose computing device which consisted of the following components except	Mill	Store	Bus	Card	C	eExam
☐	MCQ	A Bus will require how many bus lines to transfer a word of 18 bits silmutaneously	36	18	9	324	B	eExam
☐	MCQ	Karnaugh map is a convenient way of representing and simplifying _____ functions of 4 to 6 variables	Roman numerals	Boolean	Algebraic	All of the above	B	eExam
☐	MCQ	_____ is a cache writing technique in which updates are made only in the cache, setting a bit called update-bit	write block	write bits	write out	none of the above	A	eExam
☐	MCQ	Input/output modules controls the exchange between external devices and _____or external device and CPU register	cache	register	external	main memory	D	eExam
☐	MCQ	Ferrite core memory requires _____ wires	two	four	nine	five	A	eExam
☐	MCQ	The number of bits read in or out of the memory in a read or write operation is known as _____	speed rate	storage capacity	unit of transfer	access time	C	eExam
☐	MCQ	Execution of instructions in the von Neumann machine is carried out in a _____ fashion	random	sequential	dynamic	direct	B	eExam
☐	MCQ	_____ is needed in a computer to store instructions and data at the time of program execution	cache memory	auxillary memory	main memory	CD-ROM	C	eExam
☐	MCQ	Instruction is a form of ____, which supplies the information about an operation and data on which operation is to be performed	access code	control code	procedure	process	B	eExam
☐	MCQ	The basic function of a computer is the _____of a program	execution	coding	installing	develoing	A	eExam
☐	MCQ	_____ provides a path for moving data between system modules	Algorithms	topology	Data flow	Data bus	D	eExam

☐								
☐	MCQ	_____ circuits are logic circuits whose present output depends on the past inputs.	direct	Serial	Parallel	Sequential	D	eExam
☐	MCQ	which of the following characteristics of a machine does Instruction length determine?	reliability	flexibility	credibility	All of the above	B	eExam
☐	MCQ	The use of ICs in computer defined the __ generation of computers.	first	second	third	fourth	C	eExam
☐	MCQ	Register access is _____ memory access.	same speed as	slower than	faster than	none of the options	C	eExam
☐	MCQ	In _____ addressing scheme only one memory reference is required	direct	indirect	register	indexed	A	eExam
☐	MCQ	Which of the following addressing modes is used to initialise the value of a variable.	Register	Direct	Indirect	immediate	D	eExam
☐	MCQ	The advantage of _____ addressing scheme is that only a few bits are needed to address the operand	stack	register	direct	immediate	B	eExam
☐	MCQ	In programmed I/O, the I/O operations are completely controlled by the _____.	ALU	CPU	VDU	CU	B	eExam
☐	MCQ	The _____ time is the time required between the requests made for a read or write operation till the time the data is made available	cycle	response	access	waiting	C	eExam
☐	MCQ	The data bus provides a path for moving data between the system _____.	modules	instructions	program	algorithms	A	eExam
☐	MCQ	The separate lines in a system can be broadly categorised into _____ functional groups	four	two	three	five	D	eExam
☐	MCQ	The simplest model of instruction processing is a _____ process	one-step	three - step	two-step	four-step	C	eExam
☐	MCQ	_____ I/O is one in which the I/O operations are completely controlled by CPU	main memory	Interrupt driven	random memory access	Programmed	D	eExam
☐	MCQ	_____ is a sequential access device	Flash	Tape	Disk	All of the above	B	eExam

☐								
☐	MCQ	0 and 1 are the representatives of the ____ number system	Binary	Decimal	Octal	Hexadecimal	A	eExam
☐	MCQ	The decimal number system has _____ digits	Nine	Eight	Zero	Ten	D	eExam
☐	MCQ	_____ cycle is the processing needed for a single instruction	booting	Instructions	processing	Speed	A	eExam
☐	MCQ	A _____bit is an extra bit added with binary data such that it makes the total number of 1's in the data either odd or even	register	parity	processor	none of the above	B	eExam
☐	MCQ	_____ register contains data to be written in the memory	motherboard	Memory Buffer	processor	cache	B	eExam
☐	MCQ	How many types of I/O commands are available	five	three	two	four	D	eExam

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