

**NATIONAL OPEN UNIVERSITY OF NIGERIA**

**University Village, 91 Cadastral Zone, NnamdiAzikwe Expressway, Jabi, Abuja**

**FACULTY OF SCIENCES**

**NOVEMBER, 2018 EXAMINATIONS**

**COURSE CODE: CIT309**

**COURSE TITLE: Computer Architecture**

**CREDIT: 3 Units**

**TIME ALLOWED: 2½ Hours**

**INSTRUCTION: Answer Question ONE (1) and any other FOUR (4) Questions**

1a)Briefly describe what you understand by*instruction format* ***(4 marks)***

b)The most basic design issue to be faced in instruction format is its length. List the factors that effects and is affected by this decision. ***(2 marks)***

c) What is processor instruction set?***(1 mark)***

d) Enumerate the elements of a machine instruction. ***(6 marks)***

e) Source and result operands can be in one of four areas. Enumerate these areas and state when and how each are is in use.***(5 marks)***

f) Describe instruction representation in the computer. ***(4 marks)***

2a) List and write short notes on each register involved in the fetch cycle of the instruction cycle.***(5 marks)***

b) The time-shared bus is the simplest mechanism for constructing a multiprocessor system.List the components of the bus ***(1½marks)***

c) List the key design issues in multiprocessor operating design considerations.***(2½marks)***

3a) Briefly describe the taxonomy of parallel processing systems. ***(10 marks)***

b) What is process scheduling? ***(2 marks)***

4a) State the sequence of operations of the control unit in one clock pulse.***(6 marks)***

b) List and briefly explain any three (3) principal approaches to multi-threading. ***(6 marks)***

5a)List and briefly describe the common types of scheduling. ***(6 marks)***

b) Explain what is meant by a *hardwired* control unit. ***(3 marks)***

c) State and briefly explain the basic tasks performed by a micro-programmed control unit?

***(3 marks)***

6a) Brieflyexplain the five-state process model. ***(7½ marks)***

b) List and briefly describe any three features provided to facilitate DMA transfers from I/O processors in a multiprocessor system.  ***(4½ marks)***